REMARKS

Claims 1-36 are pending in the application. Claims 1, 13, and 25 are independent claims. Claims 1-36 stand rejected.

Specification

The abstract of the disclosure was objected to because the examiner contends that abstract does not support the claims.

A replacement abstract has been provided as indicated above.

Claim Rejections – 35 USC § 112

Claims 1-36 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants have amended the claims to address each claim element that the examiner found unclear. In particular, the applicants have made it more clear that the priority is associate with the cluster and with the processor.

The examiner indicates that it is unclear what a function is. Applicants respectfully disagree. The function is used in the selection of a cluster and a selection of a processor and should be accorded the meaning as understood by a person of ordinary skill in the art.

The examiner has indicated that in lines 6, 7, 10, and 13 of claim 25:

> It is not clearly indicated as to who performs the "selecting" and the "associating" steps <i.e. how could a memory alone perform a step? Is it the computer-readable instructions in line 5 that performs this?>.

Action p. 4. Applicants respectfully disagree and submit that the claim clearly indicates that it is the processor in combination with the memory and its associated computer-readable instructions that are capable of performing the selecting and associating.

Applicants submit that claims 1-36 are clear and respectfully request reconsideration of the rejection of the claims under § 112.

Claim Rejections – 35 USC § 102

Claims 1-36 stand rejected under 35 U.S.C. 102(b) as being anticipated by Kimmel et al., Patent No. 6,105,053.

Regarding claim 1, the examiner asserted that Kimmel teaches:

> selecting a first cluster from at least two clusters (Fig 1 A: all JP that routes to the same shared memory corresponds to a cluster. For example, ***JPO and JP1 make up one cluster***.),

Action p. 7. The examiner cites Kimmel as teaching the two job processors (JP0 and JP1) make up one cluster. Applicants agree that a cluster comprises more than one processor. However, next the examiner maintains that:

> each cluster having an associated priority indicator, where the selected cluster is selected as a function of its priority indicator (Col 9, lines 28-38: each node on level 1, which corresponds to a cluster, gets its own run queue. Col 6, lines 10-15, 54-61: each thread group has its own priorities. ***Each queue in all of the node levels contains the thread groups and their associated priorities***. Thus each node on level 1 will have priority values associated with it. Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47: load value for each node can be measure using priorities found in its queues, which can then be used by the scheduler perform load balancing among any nodes at any level, thus selecting a node to execute a thread group when other nodes are overloaded);

Action p. 7. As this portion of the action makes clear. The examiner finds that priority indicator in Kimmel is associated with the thread. However the claim clearly recites the opposite proposition, i.e., each cluster has an associated priority indicator. This distinction becomes more apparent when considered in the context of the remaining claim language. For example, the examiner goes on to argue that Kimmel teaches:

> selecting a first processor from the cluster, the cluster comprising at least two processors (Fig 1B, node 110 corresponds to a cluster, unit 100 and 101 are processors.), ***each processor having an associated priority indicator***, where the selected processor is selected as a function of its priority indicator (Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47);

Action p. 7. Here while the claim recites that the processor have an associated priority indicator, where that priority indicator is used to select a processor, the examiner again cites to the thread group priority indicator that is used in Kimmel to schedule and balance the execution of threads.

That priority indicator is then used in the claims to associate the processor with a set of computer-readable instructions, e.g., a thread. For example, claim 1 recites:

> associating the first processor with the first set of computer-readable instructions

Kimmel teaches the opposite.

For at least the foregoing reason, claim 1 patentably defines over Kimmel. Inasmuch as claims 2-12 incorporate the same limitations by virtue of their dependence from claim 1, Applicants submit that they also patentably define over Kimmel.

Regarding claims 13-24, the examiner provided no additional analysis and instead reiterated the analysis of claim 1:

> As per claims 13-24, they are computer-readable medium claims of claims 1-12. Therefore, they are rejected as claims 1-12 above.

Action p. 10. Accordingly, for at least the same reasons as are indicated above, Applicants submit that claims 13-24 patentably define over Kimmel.

Similarly with respect to claims 25-36, the examiner again merely reiterated the claim 1 analysis:

> Aa per claims 25-36, they are system claims of claims 1-12.
>
> Therefore, they are rejected as claims 1-12 above.

Action p. 11. Accordingly, for at least the same reasons as are indicated above, Applicants submit that claims 25-36 patentably define over Kimmel.

CONCLUSION

In the view of the foregoing amendments and remarks, Applicants respectfully submit that the present application is in condition for allowance. Reconsideration of the application and an early Notice of Allowance are respectfully requested. In the event that the Examiner cannot allow the application for any reason, the Examiner is encouraged to contact Applicants' representative.

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